

EVALUATION KIT  
AVAILABLE

MAXIM

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## General Description

The MAX8738 is an I<sup>2</sup>C-programmable VCOM-adjustment solution for thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX8738 simplifies the labor-intensive VCOM-adjustment process and replaces mechanical potentiometers, which significantly reduces labor costs, increases reliability, and enables automation.

The MAX8738 attaches to an external resistive voltage-divider and sinks a programmable current to set the VCOM voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to AVDD and is guaranteed to be monotonic over all operating conditions. This VCOM calibrator IC includes an EEPROM to store the desired VCOM voltage level. The EEPROM can be programmed repeatedly, giving TFT LCD manufacturers the flexibility to calibrate the display panel as many times as the manufacturing process requires.

The MAX8738 features a 2-wire I<sup>2</sup>C\* interface for DAC-adjustment commands and EEPROM programming. The interface utilizes the existing I<sup>2</sup>C bus on the LCD panel connector so no additional panel connector pins are required. The MAX1512 is a similar product with a 1-wire interface and is recommended for applications with no existing I<sup>2</sup>C interface.

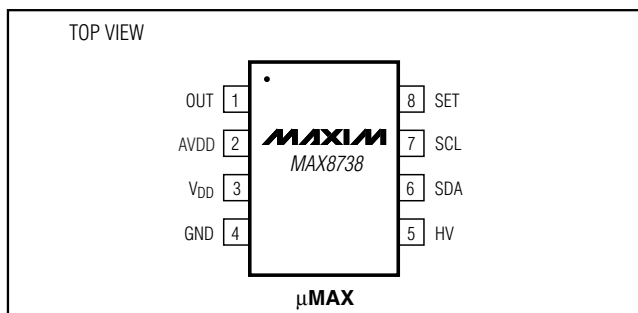
The MAX8738 is available in an 8-pin  $\mu$ MAX<sup>®</sup> package. A complete evaluation kit is available to simplify evaluation and production development.

## Applications

LCD Panels  
Notebook Computers  
Display Products  
LCD TVs

$\mu$ MAX is a registered trademark of Maxim Integrated Products, Inc.

## Pin Configuration



## Features

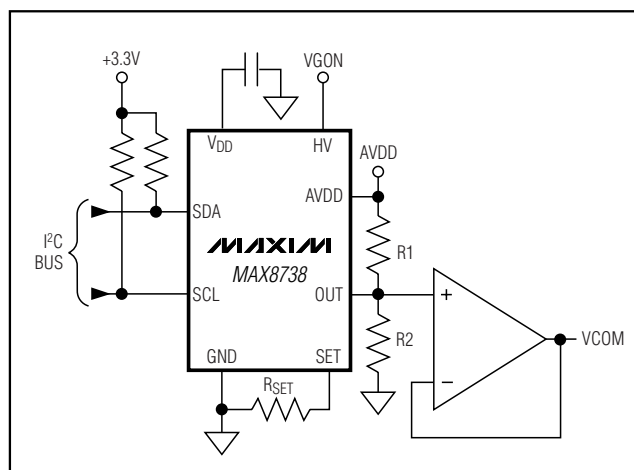
- ◆ 7-Bit Adjustable Sink-Current Output
- ◆ Resistor-Adjustable, Full-Scale Range
- ◆ Guaranteed Monotonic Output Over Operating Range
- ◆ 2-Wire I<sup>2</sup>C Interface
- ◆ EEPROM Stores VCOM Setting
- ◆ 4.5V to 20V Analog Supply Voltage Range (VAVDD)
- ◆ 60 $\mu$ A (max) AVDD Supply Current
- ◆ 16.1V to 28V EEPROM Programming Supply Voltage Range (VHV)
- ◆ <1 $\mu$ A HV Supply Current (Not in Program Mode)
- ◆ 8-Pin  $\mu$ MAX

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8738EUA	-40°C to +85°C	8 $\mu$ MAX
MAX8738EUA+	-40°C to +85°C	8 $\mu$ MAX

+ Denotes lead-free package.

## Typical Operating Circuit



Purchase of I<sup>2</sup>C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

MAXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

MAX8738

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> , SET, SCL, SDA to GND	-0.3V to +6V
OUT to GND	-0.3V to +18V
AVDD, HV to GND	-0.3V to +30V
Continuous Power Dissipation	
8-Pin $\mu$ MAX (derate 4.5mW/°C above +70°C)	362mW

Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>AVDD</sub> = 15V, V<sub>HV</sub> = 20V, V<sub>OUT</sub> = 6.75V, R<sub>SET</sub> = 30.1k $\Omega$ , T<sub>A</sub> = 0°C to +85°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SINK CURRENT ADJUSTMENT</b>						
SET Voltage Resolution			7			Bits
SET Differential Nonlinearity		Monotonic overtemperature	-1		+1	LSB
SET Zero-Scale Error			-1	+1	+2	LSB
SET Full-Scale Error			-4		+4	LSB
SET Current	I <sub>SET</sub>				120	$\mu$ A
SET External Resistance (Note 1)	R <sub>SET</sub>	To GND, V <sub>AVDD</sub> = 20V	10		200	k $\Omega$
		To GND, V <sub>AVDD</sub> = 4.5V	2.25		45.00	
V <sub>SET</sub> /V <sub>AVDD</sub> Voltage Ratio		DAC full scale		0.05		V/V
		Factory set	0.024	0.025	0.026	
<b>2-WIRE INTERFACE</b>						
Logic-Input Low Voltage	V <sub>IL</sub>	SDA, SCL			0.8	V
Logic-Input High Voltage	V <sub>IH</sub>	SDA, SCL	2.1			V
Logic-Output Low Sink Current		SDA forced to 0.4V	6			mA
Logic-Input Current		V <sub>SDA</sub> = +3.3V or GND, V <sub>SCL</sub> = +3.3V or GND	-1		+1	$\mu$ A
SDA and SCL Input Capacitance		SDA, SCL		5		pF
SCL Frequency	f <sub>CLK</sub>		DC		100	kHz
SCL High Time	t <sub>CLH</sub>		4000			ns
SCL Low Time	t <sub>CLL</sub>		4700			ns
SDA and SCL Rise Time	t <sub>R</sub>	(Note 2)			1000	ns
SDA and SCL Fall Time	t <sub>F</sub>	(Note 2)			300	ns
START Condition Hold Time	t <sub>HDSTT</sub>	10% of SDA to 90% of SCL	4000			ns
START Condition Setup Time	t <sub>SUSTT</sub>		4700			ns
Data Input Hold Time	t <sub>HDDAT</sub>		0			ns
Data Input Setup Time	t <sub>SUDAT</sub>		250			ns
STOP Condition Setup Time	t <sub>SUSTP</sub>		4000			ns
Bus Free Time	t <sub>BF</sub>		4700			ns
Input Filter Spike Suppression	t <sub>SP</sub>	SDA, SCL (Note 2)		1		$\mu$ s
<b>V<sub>DD</sub> REGULATOR</b>						
V <sub>DD</sub> Output Voltage	V <sub>DD</sub>	4.5V < V <sub>AVDD</sub> < 20V, I <sub>VDD</sub> = 0	3.1	3.6	4.5	V
V <sub>DD</sub> Power-On Reset Threshold		Rising edge, 100mV hysteresis			3.0	V

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

**MAX8738**

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>AVDD</sub> = 15V, V<sub>HV</sub> = 20V, V<sub>OUT</sub> = 6.75V, R<sub>SET</sub> = 30.1kΩ, T<sub>A</sub> = 0°C to +85°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AVDD SUPPLY</b>						
AVDD Supply Range	V <sub>AVDD</sub>		4.5		20.0	V
AVDD Operating Current	I <sub>AVDD</sub>	V <sub>AVDD</sub> = 20V		25	60	μA
<b>HV SUPPLY</b>						
HV Input Voltage Range	V <sub>HV</sub>		16.1		28.0	V
HV Power-On Reset Threshold		Rising edge, 60mV hysteresis		15.6	16.0	V
HV Input Bias Current	I <sub>HV</sub>	Not in program mode (Note 3)		0.1	1	μA
		Program mode (Note 3)		15	30	
		During program (Note 4)			60	
<b>OUTPUT VOLTAGE</b>						
OUT Leakage Current				±100		nA
OUT Settling Time		To ±0.5 LSB error band		20		μs
OUT Voltage Range	V <sub>OUT</sub>		V <sub>SET</sub> + 0.5V		13	V

## ELECTRICAL CHARACTERISTICS

(V<sub>AVDD</sub> = 15V, V<sub>HV</sub> = 20V, V<sub>OUT</sub> = 6.75V, R<sub>SET</sub> = 30.1kΩ, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Figure 1) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SINK CURRENT ADJUSTMENT</b>						
SET Differential Nonlinearity		Monotonic overtemperature	-1		+1	LSB
SET Zero-Scale Error			-1		+2	LSB
SET Full-Scale Error			-4		+4	LSB
SET Current	I <sub>SET</sub>				120	μA
SET External Resistance (Note 1)	R <sub>SET</sub>	To GND, V <sub>AVDD</sub> = 20V	10		200	kΩ
		To GND, V <sub>AVDD</sub> = 4.5V	2.25		45.00	
<b>2-WIRE INTERFACE</b>						
Logic-Input Low Voltage	V <sub>IL</sub>	SDA, SCL			0.8	V
Logic-Input High Voltage	V <sub>IH</sub>	SDA, SCL	2.1			V
Logic-Output Low Sink Current		SDA forced to 0.4V	6			mA
Logic-Input Current	I <sub>LI</sub>	V <sub>SDA</sub> = +3.3V or GND, V <sub>SCL</sub> = +3.3V or GND	-1		+1	μA
SCL Frequency	f <sub>CLK</sub>		DC		100	kHz
SCL High Time	t <sub>CLH</sub>		4000			ns
SCL Low Time	t <sub>CLL</sub>		4700			ns
SDA and SCL Rise Time	t <sub>R</sub>	(Note 2)			1000	ns
SDA and SCL Fall Time	t <sub>F</sub>	(Note 2)			300	ns

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>AVDD</sub> = 15V, V<sub>HV</sub> = 20V, V<sub>OUT</sub> = 6.75V, R<sub>SET</sub> = 30.1kΩ, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Figure 1) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Hold Time	t <sub>HDSTT</sub>	10% of SDA to 90% of SCL	4000			ns
START Condition Setup Time	t <sub>SUSTT</sub>		4700			ns
Data Input Hold Time	t <sub>HDDAT</sub>		0			ns
Data Input Setup Time	t <sub>SUDAT</sub>		250			ns
STOP Condition Setup Time	t <sub>SUSTP</sub>		4000			ns
Bus Free Time	t <sub>BF</sub>		4700			ns
<b>V<sub>DD</sub> REGULATOR</b>						
V <sub>DD</sub> Output Voltage	V <sub>DD</sub>	4.5V < V <sub>AVDD</sub> < 20V, I <sub>VDD</sub> = 0	3.1		4.5	V
V <sub>DD</sub> Power-On Reset Threshold		Rising edge, 100mV hysteresis			3.0	V
<b>AVDD SUPPLY</b>						
AVDD Supply Range	V <sub>AVDD</sub>		4.5		20.0	V
AVDD Operating Current	I <sub>AVDD</sub>	V <sub>AVDD</sub> = 20V			60	μA
<b>HV SUPPLY</b>						
HV Input Voltage Range	V <sub>HV</sub>		16.1		28.0	V
HV Power-On Reset Threshold		Rising edge, 60mV hysteresis			16.0	V
HV Input Bias Current	I <sub>HV</sub>	Not in program mode (Note 3)			1	μA
		Program mode (Note 3)			30	
		During program (Note 4)			60	
<b>OUTPUT VOLTAGE</b>						
OUT Voltage Range	V <sub>OUT</sub>		V <sub>SET</sub> + 0.5V		13	V

**Note 1:** SET resistors are only checked at full scale.

**Note 2:** Guaranteed by design. Not production tested.

**Note 3:** The MAX8738 enters program mode after any valid command is received, except the AAh command.

**Note 4:** Program time lasts for 11ms.

**Note 5:** Specifications from 0°C to -40°C are guaranteed by design, not production tested.

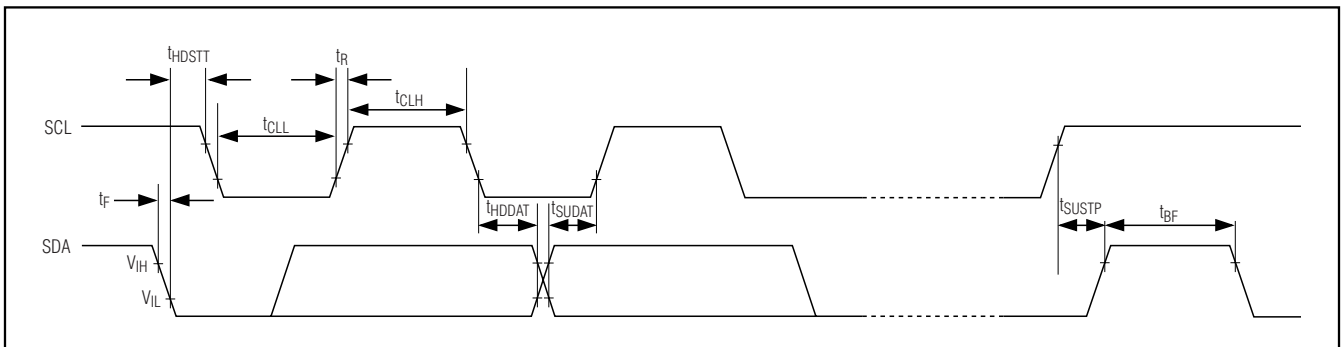


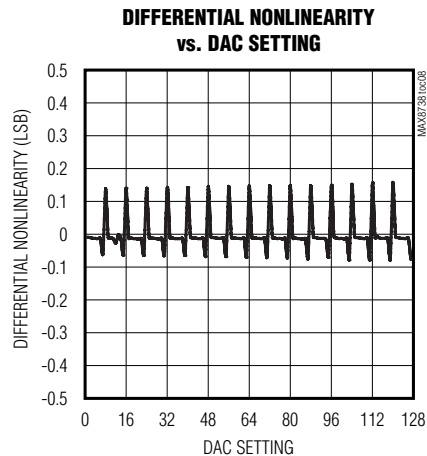
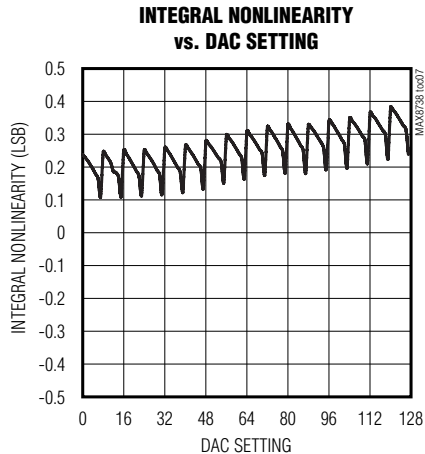
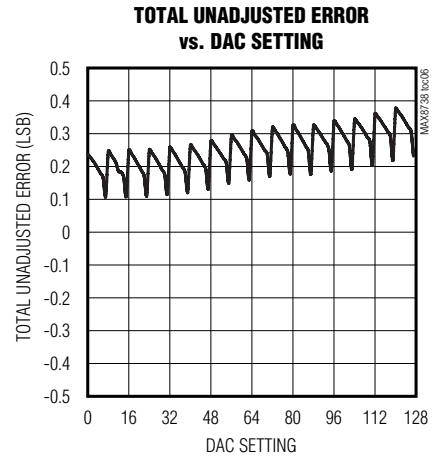
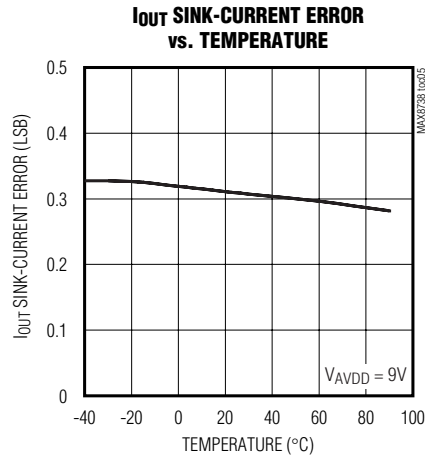
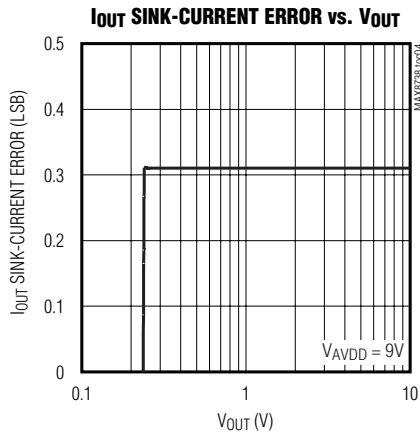
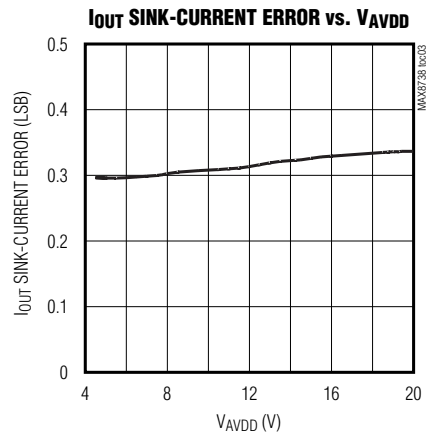
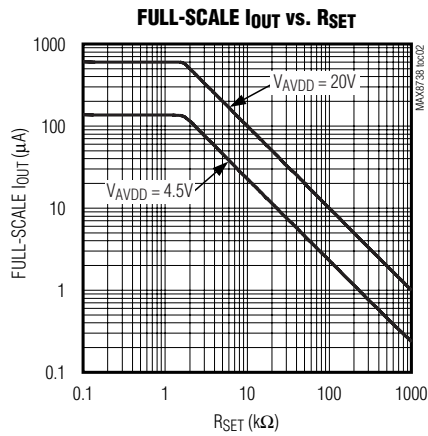
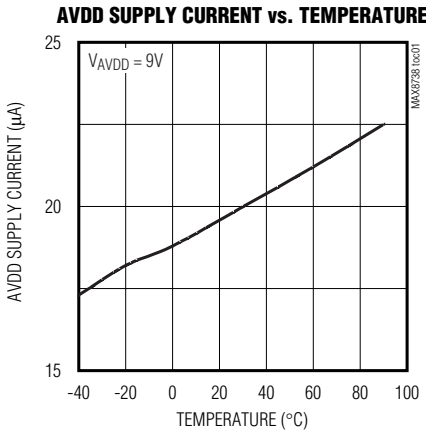
Figure 1. Timing Definitions Used in the Electrical Characteristics

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## Typical Operating Characteristics

(V<sub>AVDD</sub> = 9V, V<sub>HV</sub> = 18V, R<sub>SET</sub> = 24.9kΩ, T<sub>A</sub> = +25°C, unless otherwise noted.)

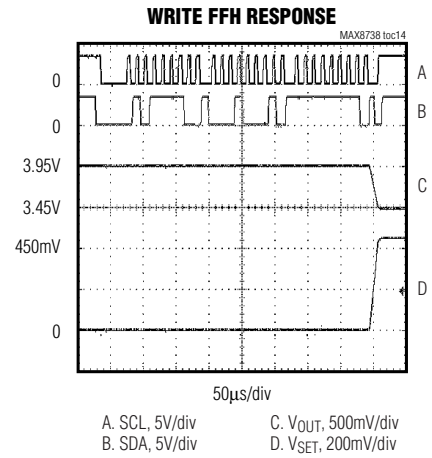
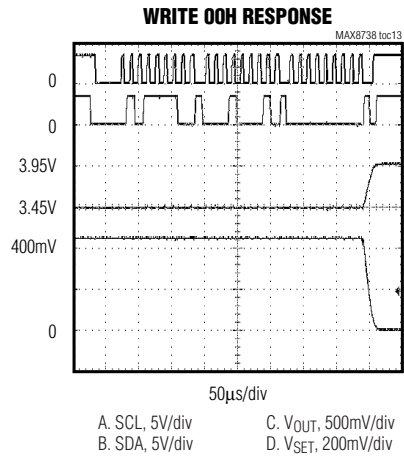
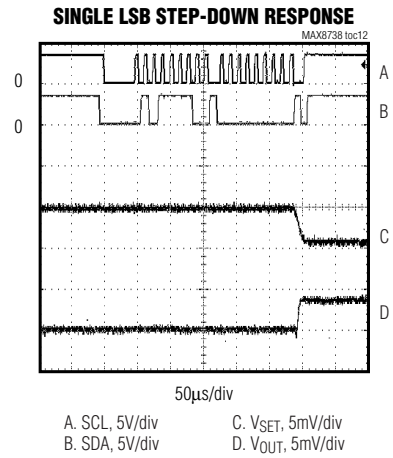
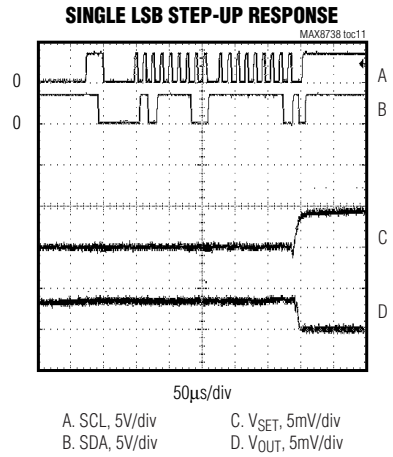
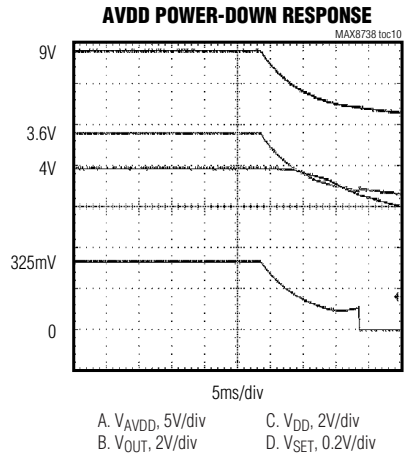
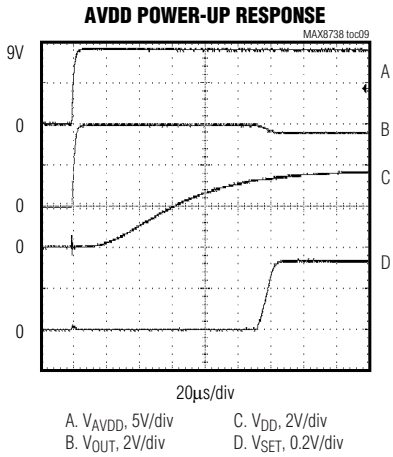
MAX8738



# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## Typical Operating Characteristics (continued)

(V<sub>AVDD</sub> = 9V, V<sub>HV</sub> = 18V, R<sub>SET</sub> = 24.9kΩ, T<sub>A</sub> = +25°C, unless otherwise noted.)



# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

**MAX8738**

## Pin Description

PIN	NAME	FUNCTION
1	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider between AVDD and GND that sets the VCOM voltage. I <sub>OUT</sub> lowers the divider voltage by an adjustable amount. See the SET pin description.
2	AVDD	High-Voltage Analog Supply. Bypass to GND with a 0.1μF capacitor.
3	V <sub>DD</sub>	3.6V Regulator Output. V <sub>DD</sub> provides the supply voltage to the entire IC. V <sub>DD</sub> is not for external use. Bypass to GND with a 0.1μF capacitor.
4	GND	Ground. Connect to system ground.
5	HV	EEPROM High-Voltage Programming Supply. Bypass to GND with a 0.1μF capacitor. Connect this pin to the TFT LCD VGON supply. VGON should be between 16.1V and 28V. The HV pin supplies the power for the internal EEPROM writing cycle. The internal writing circuits are disabled when HV is less than 15.6V (typ).
6	SDA	I <sup>2</sup> C-Compatible Clock Input
7	SCL	I <sup>2</sup> C-Compatible Serial Bidirectional Data Line
8	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R <sub>SET</sub> , from SET to GND to set the full-scale adjustable sink current. The full-scale adjustable sink current is equal to: $\left( \frac{V_{AVDD}}{20 \times R_{SET}} \right)$ I <sub>OUT</sub> is equal to the current through R <sub>SET</sub> .

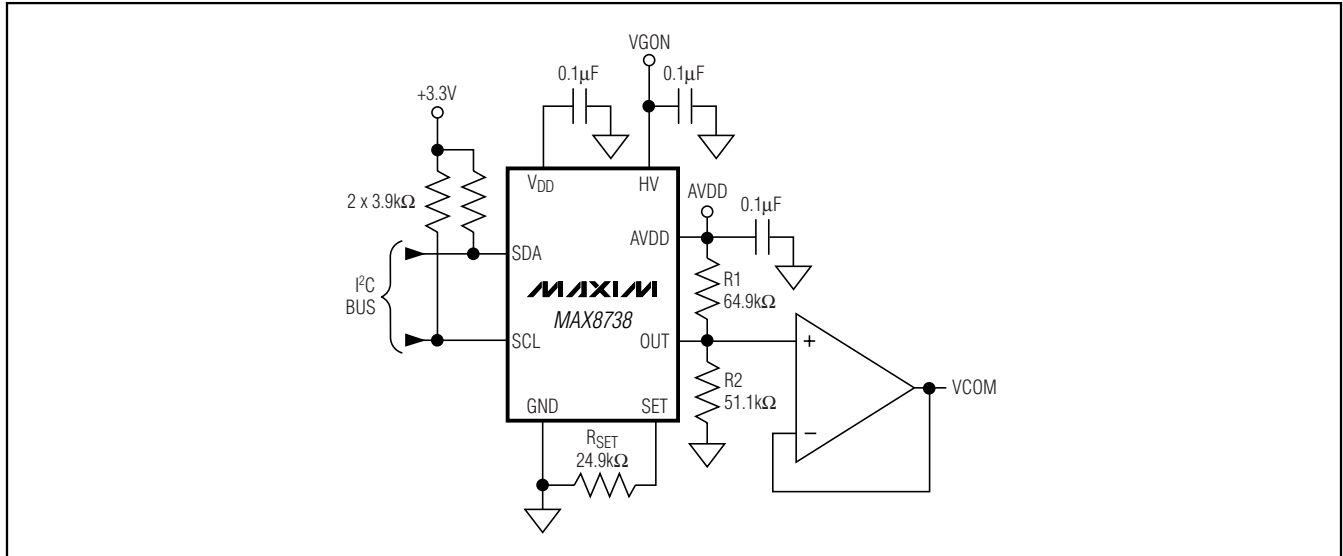


Figure 2. Standard Application Circuit

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

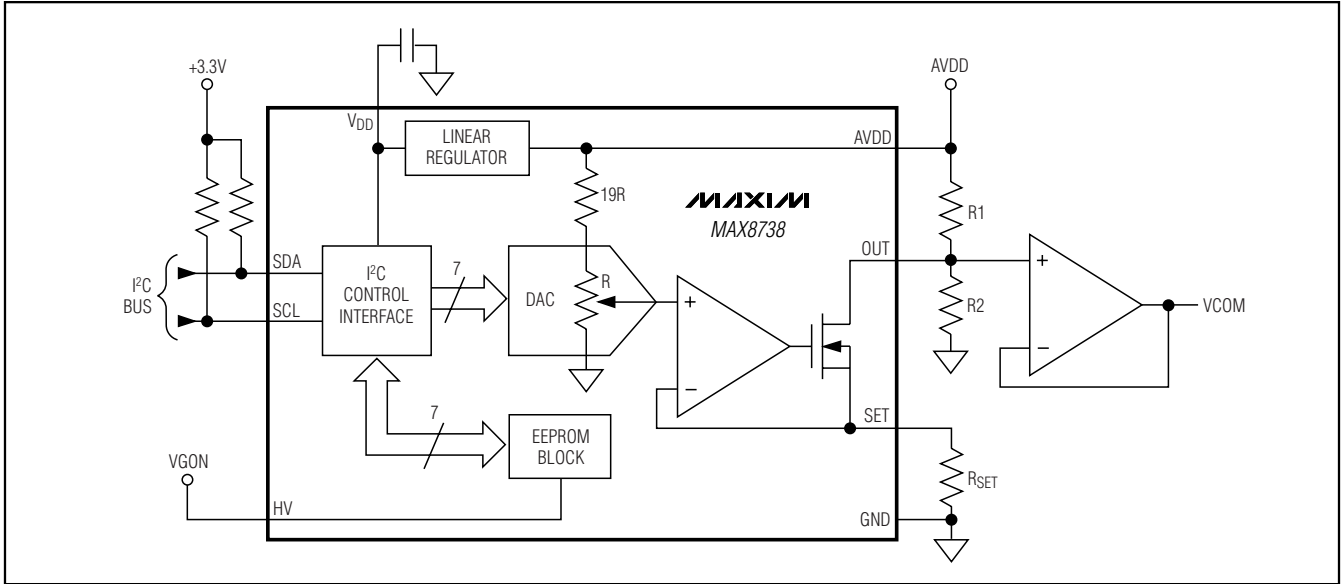


Figure 3. Simplified Functional Diagram

## Detailed Description

The MAX8738 is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. The MAX8738 attaches to an external resistive voltage-divider and sinks a programmable current (I<sub>OUT</sub>), which sets the VCOM level (Figure 2). An internal 7-bit DAC controls the sink current and allows the user to increase or decrease the VCOM level (Figure 3). The DAC is ratio-metric relative to V<sub>AVDD</sub> and is monotonic over all operating conditions. The user can store the DAC setting in an internal EEPROM. On power-up, the EEPROM presets the DAC to the last stored setting. The 2-wire I<sup>2</sup>C interface between the LCD panel and the programming circuit adjusts the DAC and programs the EEPROM.

The resistive voltage-divider and the AVDD supply set the maximum value of VCOM. The MAX8738 sinks current from the voltage-divider to reduce the VCOM level. The external resistor R<sub>SET</sub> sets the full-scale sink current and the minimum value of VCOM.

### Supply Voltages

#### AVDD and VDD

The MAX8738 has an internal linear regulator that generates a 3.6V VDD voltage from the AVDD supply voltage. The VDD voltage supplies power to the MAX8738 and should not be used for external loads. AVDD accepts voltages from 4.5V to 20V. Bypass AVDD and VDD to GND with a 0.1μF capacitor each.

### HV

The HV input provides the high voltage required to program the EEPROM. The HV pin is typically connected to the TFT LCD positive gate driver supply (VGON) supply. VGON should be between 16.1V and 28V. EEPROM programming is disabled when HV is below 15.6V (typ). Bypass HV to GND with a 0.1μF capacitor.

The EEPROM programming block is turned off when the MAX8738 first powers up, and also immediately after the EEPROM is programmed. When the EEPROM programming block is off, the HV supply current is less than 1μA.

After the MAX8738 receives any command that changes the DAC value, the EEPROM programming block is enabled, and the HV supply current increases to 15μA (typ). During the programming of the EEPROM, the HV supply current may draw up to 60μA (max).

### Setting the VCOM Adjustment Range (R<sub>SET</sub>)

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R<sub>SET</sub> sets the full-scale sink current, I<sub>OUT</sub>, which determines the minimum value of the VCOM adjustment range. Large R<sub>SET</sub> values increase resolution but decrease the VCOM adjustment range. Calculate R<sub>1</sub>, R<sub>2</sub>, and R<sub>SET</sub> using the following procedure:



# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

- 1) Choose the maximum VCOM level (V<sub>MAX</sub>), the minimum VCOM level (V<sub>MIN</sub>), and the AVDD supply voltage (V<sub>AVDD</sub>).
- 2) Select R1 between 10kΩ and 500kΩ based on the acceptable power loss from the AVDD supply rail.
- 3) Calculate R2:

$$R2 \cong \frac{V_{MAX}}{(V_{AVDD} - V_{MAX})} \times R1$$

- 4) Calculate R<sub>SET</sub>:

$$R_{SET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R1$$

- 5) Verify that I<sub>SET(MAX)</sub> does not exceed 120μA:

$$I_{SET(MAX)} = \frac{V_{AVDD}}{20 \times R_{SET}} \leq 120\mu A$$

- 6) If I<sub>SET</sub> exceeds 120μA, return to step 2 and choose a larger value for R1.

- 7) The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

- 1) V<sub>MAX</sub> = 5V, V<sub>MIN</sub> = 3V, V<sub>AVDD</sub> = 10V.
- 2) If R1 = 200kΩ, then R2 = 200kΩ and R<sub>SET</sub> = 24.9kΩ.
- 3) I<sub>SET(MAX)</sub> = 20μA.
- 4) Resolution = 15.75mV.

### Translating Existing Potentiometer Circuits

Existing VCOM adjustment circuits using conventional mechanical potentiometers can be translated into MAX8738 circuits. Figures 4 and 5 show two common adjustment circuits and their equivalent MAX8738 circuits.

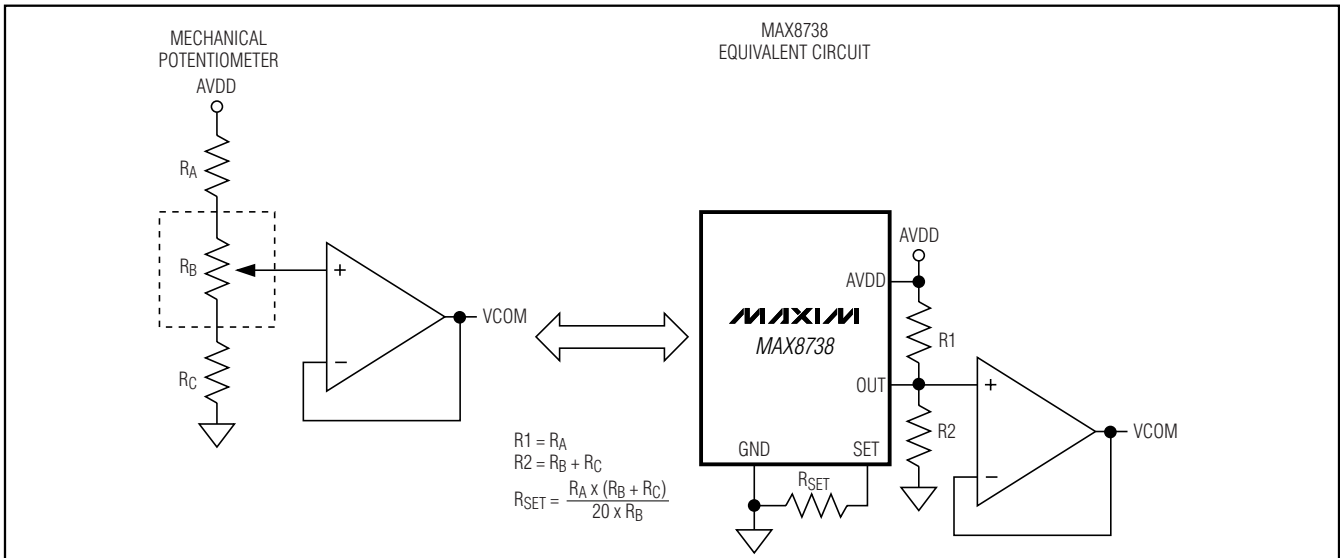


Figure 4. Replacement of Mechanical Potentiometer Circuit

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

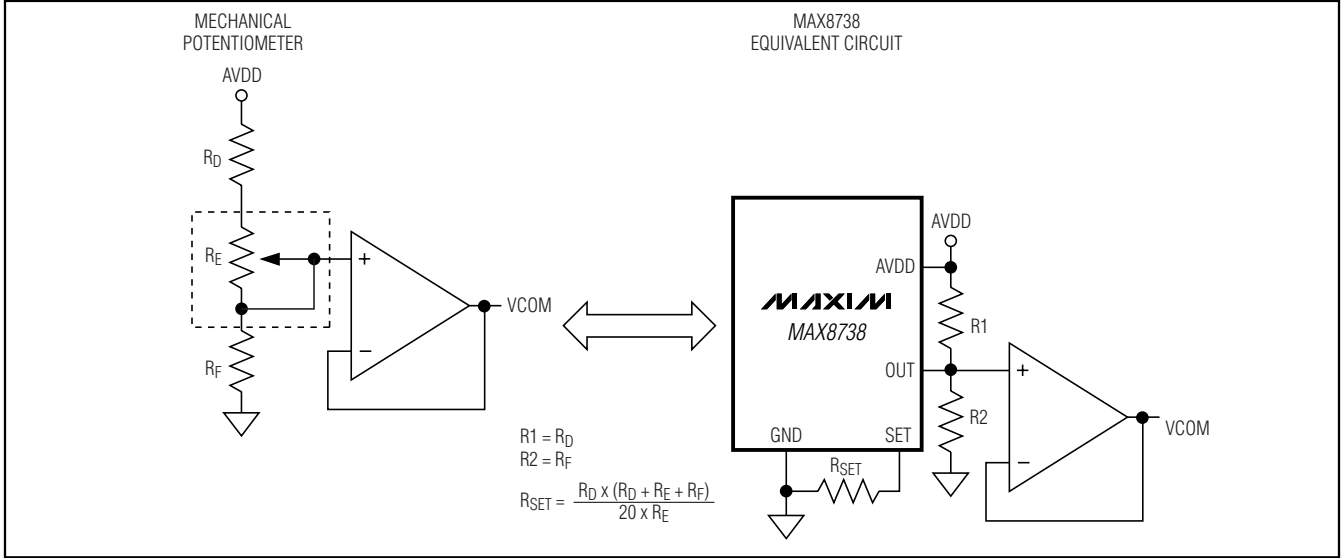


Figure 5. Replacement of Mechanical Potentiometer Circuit

## Applications Information

### I<sup>2</sup>C-Bus-Compatible Interface

The MAX8738 is a receive-only device with an I<sup>2</sup>C address of 5Eh. The 2-wire, I<sup>2</sup>C-bus-compatible serial interface (pins SCL and SDA) is designed to attach to a I<sup>2</sup>C bus. Connect both SCL and SDA lines to the positive bus supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \leq \frac{t_R}{C_{BUS}}$$

where  $t_R$  is the rise time in the *Electrical Characteristics*, and  $C_{BUS}$  is the total capacitance on the bus.

The MAX8738 is compatible with the standard I<sup>2</sup>C interface protocol as defined in the following subsections. See Figure 6.

### Bus Not Busy

The I<sup>2</sup>C bus is not busy when both data and clock lines remain HIGH. Data transfers may be initiated only when the bus is not busy.

### START Data Transfer (S)

Starting from an idle bus state (both SDA and SCL are high), a START condition consists of a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH. All commands must be preceded by a START condition.

### STOP Data Transfer (P)

A STOP condition consists of a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH. All operations must be ended with a STOP condition.

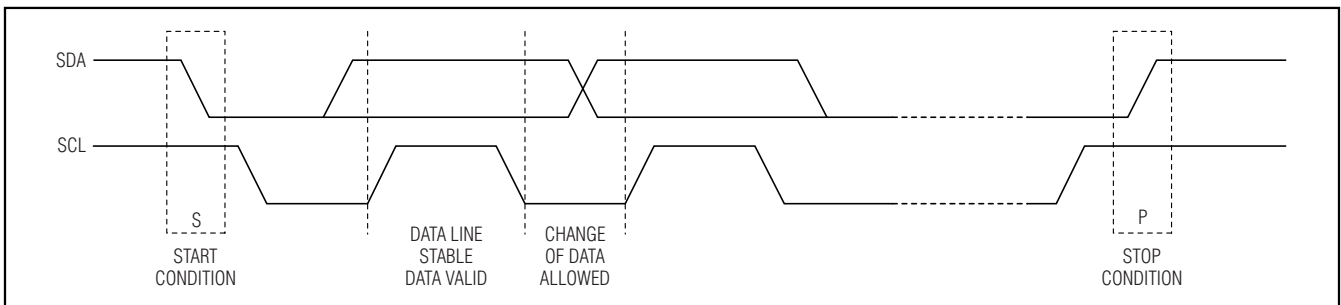


Figure 6. I<sup>2</sup>C Bus START, STOP, and Data Change Conditions

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

### Slave Address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (0b0101111 or 5Eh) for the MAX8738. Since the MAX8738 is a write-only device, the eighth bit of the slave address is zero. The MAX8738 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit when it recognizes its address.

### SDA Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

### Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each

byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. See Figure 7.

The MAX8738 does not acknowledge the program EEPROM command (AAh) if HV is below 15.6V (typ) or if the MAX8738 is not in program mode.

The MAX8738 does not acknowledge any command while an internal programming cycle is in progress. Once the internally timed EEPROM write cycle has started, acknowledge polling can be initiated. This involves repeatedly sending a 55h command. Only if the internal write cycle has completed does the MAX8738 acknowledge the command.

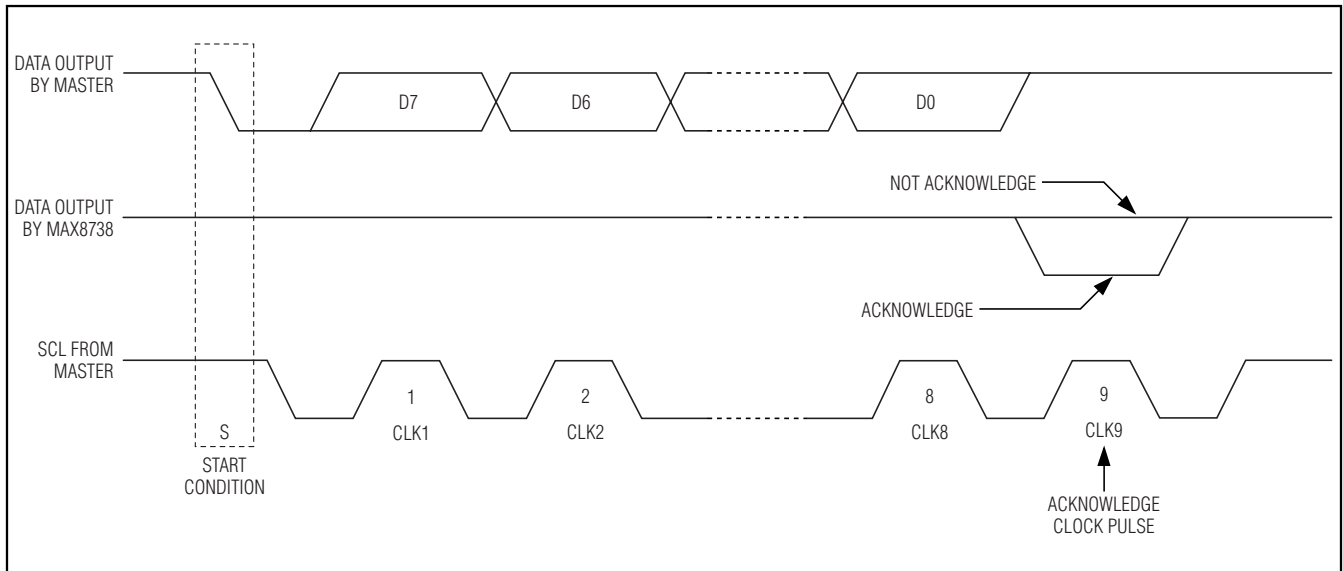


Figure 7. I<sup>2</sup>C Bus Acknowledge

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

**Table 1. Command Byte Functions**

BYTE	FUNCTION	FIGURE
00h	Decrement the DAC setting by 1 LSB	8A
FFh	Increment the DAC setting by 1 LSB	8A
AAh	Write the current DAC setting to EEPROM	8A
55h	Load the EEPROM setting to the DAC	8A
11h	Write a specific value to the DAC	8B

### Command Byte

A complete command consists of a START condition (S) followed by the MAX8738's slave address (5Eh) and a command byte, or a command byte and a DAC value, followed by a STOP condition (P). There are five commands, and their functions are listed in Table 1.

### DAC Values

Table 2 lists the DAC values and the corresponding ISET, VSET, and VOUT values.

### Layout Information

Use the following guidelines for good layout:

- 1) Place the VCOM buffer and the R1/R2 voltage-divider close to the OUT pin (Figure 2).
- 2) Place RSET close to SET.

**Table 2. DAC Settings**

DAC VALUE	ISET	VSET (V)	VOUT (V)
FFh	ISET(MAX)	VSET(MAX)	V <sub>MIN</sub>
FEh	ISET(MAX) - 1 LSB	VSET(MAX) - 1 LSB	V <sub>MIN</sub> + 1 LSB
.	.	.	.
.	.	.	.
.	.	.	.
01h	ISET(MIN) + 1 LSB	VSET(MIN) + 1 LSB	V <sub>MAX</sub> - 1 LSB
00h	ISET(MIN)	VSET(MIN)	V <sub>MAX</sub>

- 3) Bypass V<sub>DD</sub> and AV<sub>DD</sub> with 0.1μF capacitors placed close to the IC with short connections to the pins.
- 4) Refer to the MAX8738 evaluation kit for an example of proper board layout.

### Chip Information

TRANSISTOR COUNT: 6198

PROCESS: BiCMOS

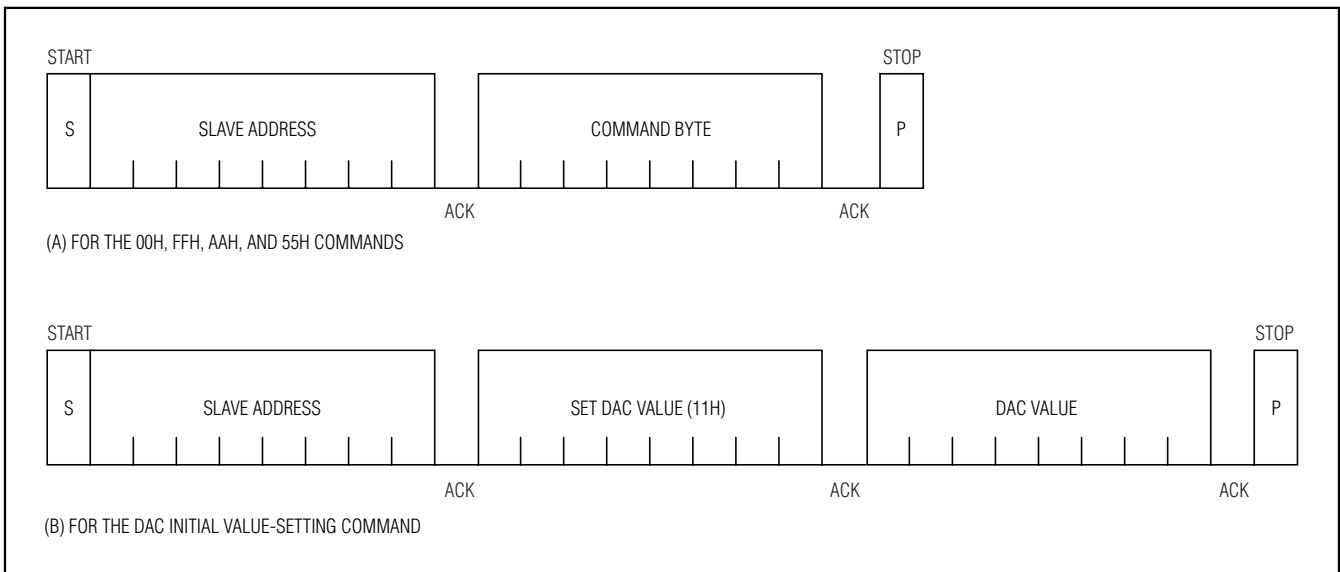


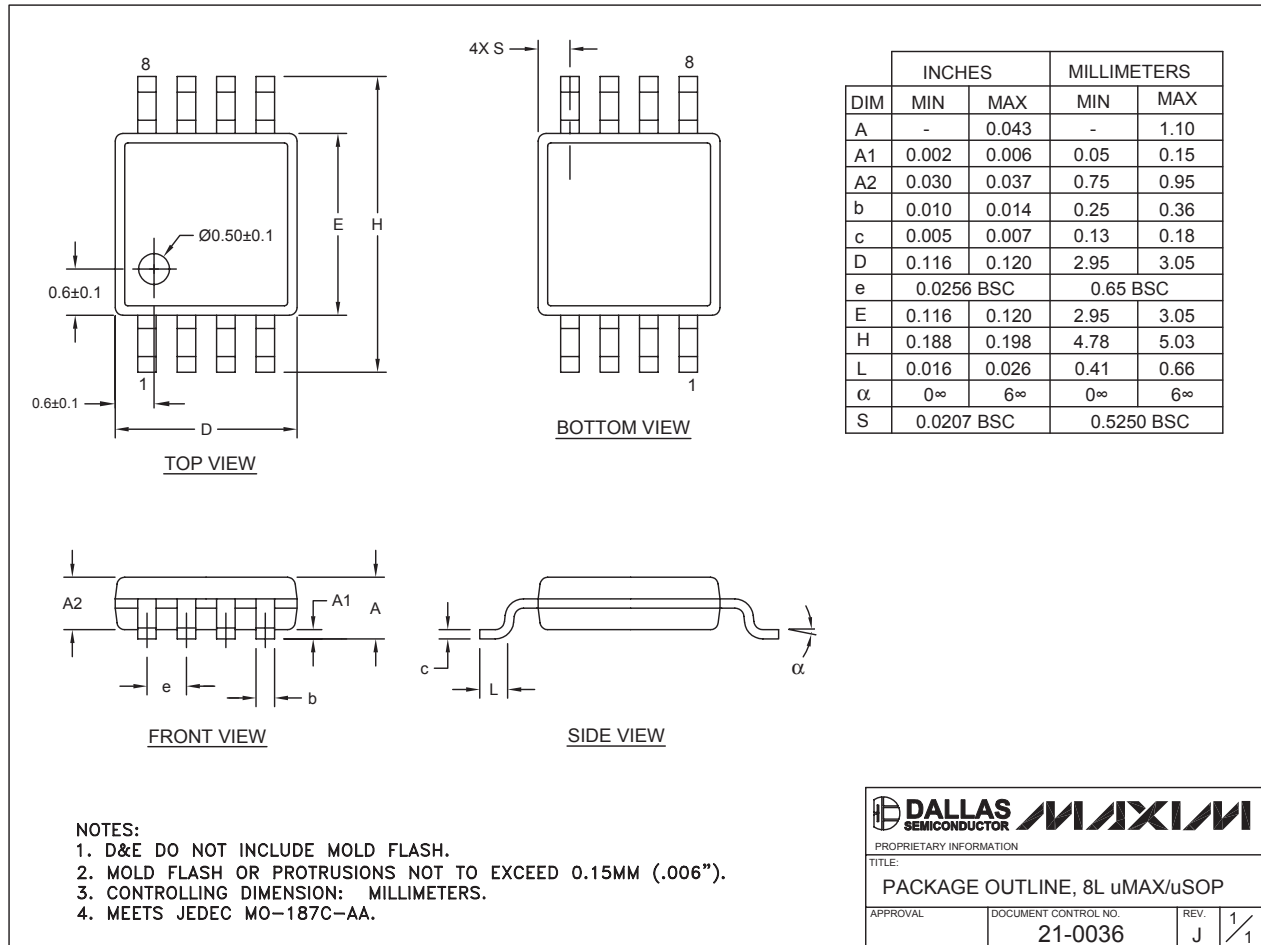
Figure 8. I<sup>2</sup>C Bus Data Transfer Summary

# EEPROM-Programmable TFT VCOM Calibrator with I<sup>2</sup>C Interface

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX8738



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 13